FPGA based sliding mode control for high frequency SEPIC

Nan Li, Xuefang Lin-Shi, Pierre Lefranc, Emmanuel Godoy, Ali Jaafar

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N. Li[1], X. Lin-Shi[1], P. Lefranc[2], E. Godoy[3], A. Jaafar[3],
1. AMPERE Laboratory, CNRS UMR 5005, INSA-Lyon, Villeurbanne, France
linan400@126.com, xuefang.shi@insa-lyon.fr
2. Energy Systems Department, SUPELEC, Gif sur Yvette, France
Pierre.Lefranc@supelec.fr
3. Automatic Control Department, SUPELEC, Gif sur Yvette, France
Emmanuel.Godoy@supelec.fr, Ali.Jaafar@supelec.fr

Abstract: **This paper presents the application of fixed frequency (or indirect) Sliding Mode Control (SMC) to the DC-DC Single-Ended Primary Inductor Converter (SEPIC) where the switching frequency is in the range of hundreds of kHz and consequently a FPGA is required. Due to the constraint of FPGA, only the output voltage is measured. As the proposed SMC requires the knowledge of all the states, an extended Kalman observer is introduced to estimate the state vector and the load variation. A multi-bit second-order Δ-Σ modulator is used to effectively achieve 11-bit resolution at high-frequency through only a 8-bit hardware Core Digital Pulse – Width -Modulator (DPWM). Simulation and experimental studies are conducted for a laboratory prototype with switching frequency of 500 kHz. Results proved the performance of the proposed solution.**

Index Terms: Power converters, SEPIC, sliding mode control, extended Kalman filter, DPWM, FPGA implementation.

I. INTRODUCTION

Digital controller has become recently an attractive candidate in monolithic integrated switching-mode power supplies (SMPS) for high performance applications due to their well-known advantages. Compared to analog control [1], digital implementation is less sensitive to environment because of elimination of component tolerance and aging. Moreover digital control enables to implement more sophisticated control strategies to improve system dynamic performances. In addition, using the available automated design soft tools, digital controller design cycle can be accelerated, and offers a degree of programming flexibility. The continuous increase of SMPS applications requiring DC-DC converters operating in both step-up and step-down modes with high efficiency and precision has encouraged the study of complex circuit topologies. Simple topologies like Buck, Boost and Buck-Boost being insufficient for such demands, more complex converters, like the SEPIC (Single-Ended Primary Inductor Converter), shown in Fig. 1, are of great interest to fulfill these requirements, which could lead to the design of a "universal DC-DC converter". The SEPIC provides several advantages of which being a step up/down converter and having the control switch connected to the ground. The main drawback is that it is a nonlinear fourth order system which renders its control more complicated [2].

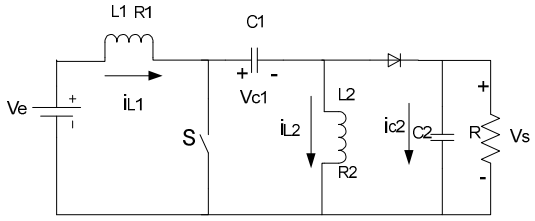


Fig. 1: Circuit diagram of the SEPIC converter

Sliding Mode Control (SMC) is a nonlinear control one [3] used in many applications especially in nonlinear systems with variable structures. As most control methods, SMC has been widely studied on basic DC-DC converters such as the Buck, Boost, and Buck-Boost converters [4], [5], [6]. More complex converters were also studied [7], [8], [9], [10], [11], [12]. Generally DSP systems are used to implement SMC. DSP or DSPIC systems present sufficient resources to accommodate the modest switching frequency of the converter in the range of kHz. However, in embedded applications, switching frequencies in the range of hundreds of kHz or MHz are necessary in order to reduce the size of passive components. DSP and DSPIC solutions have limited frequency or are unrealistic for commercial applications, where faster processing devices such as FPGA or ASIC are required. To our knowledge, the studies of a SEPIC with a digital Sliding Mode (SM) controller operating at high-frequency have not been reported yet.

This paper presents a combination design of indirect SMC and a multi-bit second-order Δ-Σ modulator DPWM for FPGA implementation. The paper is organized as following: Section 2 illustrates the principle of the indirect SMC and the ways of applying this control to SEPIC converter. In section 3, two double-integral SM controllers are proposed and compared on simulation. In section 4, an Extended Kalman Filter (EKF) is developed to estimate the state vector and the load variation. The FPGA implementation of whole SMC, EKF and DPWM is presented in section 5.

II. INDIRECT SM CONTROLLER

There are two main types of SMC strategies applied to power converters: Hysteresis-Modulation-Based SM Controllers [13] and indirect SM Controllers [14]. The first

type of SMC has generally not constant switching frequency. Operating a DC-DC converter at a variable frequency is not preferred. It has been shown that HM-based SM-controlled converters generally suffer from significant switching-frequency variation when the input voltage and the output load are varied [13], [15]. This complicates the design of the input and output filters. Obviously, designing the filters under a worst case (lowest) frequency condition will result in oversized filters. Moreover, the variation of the switching frequency also deteriorates the regulation properties of the converters.

In the indirect SM Controllers case, the control signal is continuous and derived based on the equivalent control as follows:

Let: $\dot{x} = A(x,t) + B(x,t)u$ and $s(x) = K^T x$, then

$$\dot{s}(x) = 0 \text{ gives } u_{eq} = -(K^T B)^{-1} K^T A \quad (1)$$

where $s(x)$ is the sliding surface. The vector x can be the state vector itself or a vector whose elements are a combination of the states, which in this case is called control vector. For power converters, u_{eq} is the duty cycle ρ, provided that the switching frequency is relatively large [13], thus the converter is controlled here by varying the duty cycle and keeping the switching frequency constant. In our work, we will study the equivalent control on the SEPIC.

III. DOUBLE-INTEGRAL SLIDING MODE CONTROLLER

DC-DC converter modeling has been widely studied through the past decades [16]. The digital control system in sliding mode has been successfully applied to simple DC-DC Buck converter [17]. For the application of SMC to the SEPIC, a nonlinear averaged state space representation is suitable.

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{v}_{c1} \\ \dot{i}_{L2} \\ \dot{v}_s \end{bmatrix} = \begin{bmatrix} -\frac{R_1}{L_1} & \frac{\rho-1}{L_1} & 0 & \frac{\rho-1}{L_1} \\ \frac{1-\rho}{C_1} & 0 & \frac{\rho}{C_1} & 0 \\ 0 & -\frac{\rho}{L_2} & -\frac{R_2}{L_2} & \frac{1-\rho}{L_2} \\ \frac{1-\rho}{C_2} & 0 & \frac{\rho-1}{C_2} & -\frac{1}{C_2 R} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{c1} \\ i_{L2} \\ v_s \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_e] \quad (2)$$

where R_1 and R_2 are the ESRs of the inductors L_1 and L_2 respectively and representing the circuit losses, v_e is the input voltage and the ρ is the duty cycle of the switch.

As previously mentioned, the sliding surface is taken as a linear combination of the state variables or of the control vector elements. Although there are infinite possibilities for choosing the surface, nonlinear combinations give complex control laws that cannot be often physically realized. The highest number of state variables present in $s(x)$ in the case of the SEPIC is four since the system is of fourth order; however, this induces four control parameters that must be systematically chosen. The control objective is to keep the output voltage Vs tracking the reference voltage Vref. In [18], it has been shown that a PID-surface [19] given by:

$$s = \lambda_1 e_1 + \lambda_2 \frac{de_1}{dt} + \lambda_3 \int e_1 dt \text{ with } e_1 = V_{ref} - v_s \quad (3)$$

would give an unstable control law for the SEPIC. An Integral Sliding Mode Controller (ISMC) is proposed in [20] as follow:

$$s = \alpha_1 e_1 + \alpha_2 e_2 + \alpha_3 \int [e_1 + e_2] dt \text{ with } e_2 = i_{ref} - i_{L1} \quad (4)$$

where i_{ref} denote the reference current which can be taken as $K[V_{ref} - v_s]$ with K the amplified gain of the voltage error. This control gives better dynamics than a classical PI control. Unfortunately it can not fully alleviate the steady-state error of the output voltage [20].

In this paper, an additional double-integral term of the output voltage is added in the sliding surface (4). The sliding surface is defined as:

$$s = \beta_1 e_1 + \beta_2 e_2 + \beta_3 \int [e_1 + e_2] dt + \beta_4 \int \int (e_1 dt) dt \quad (5)$$

where β_1, β_2, β_3 and β_4 represent the control parameters termed as sliding coefficients.

The duty cycle expression (equivalent control) is found to be:

$$\begin{cases} \rho = \frac{1}{v_{c1} + v_s} [K_1 (V_{ref} - v_s) + K_4 \int (V_{ref} - v_s) dt - K_3 i_{L1} \\ -K_2 i_{c2} + R_1 i_{L1} + (v_{c1} + v_s - v_e)] \end{cases} \quad (6)$$

where $K_1 = \frac{\beta_3}{\beta_2} L_1 (K+1), K_2 = \frac{1}{C_2} L_1 \left(K + \frac{\beta_1}{\beta_2} \right), K_3 = \frac{\beta_3}{\beta_2} L_1, K_4 = \frac{\beta_4}{\beta_2} L_1$ are the adjustable parameters in this so-called Double Integral Sliding Mode Controller (DISMC).

The ranges of employable gain parameters K_1, K_2, K_3 and K_4 for the controller design can be found by deriving the existence condition. We will find the regions of attraction which are imposed by the SMC strategy. For this purpose, the local reachability condition $\lim_{e \to 0} s\dot{s} < 0$ must be satisfied.

One solution is to compute the regions of attraction in terms of these parameters and then choose them in such a way that the regions cover all the expected range of operation of the converter. Any present state variable is replaced with either its upper or lower bound depending on the inequality. Thus, we get from a system of inequalities in K_1, K_2, K_3 and K_4:

$$\begin{cases} V_{e(\min)} - K_1 [V_{ref} - v_{ss}] - K_4 \int [V_{ref} - v_{ss}] dt \\ + K_2 i_{c2(\min)} - (K_3 - R_1) i_{L1(\min)} > 0 \\ V_{e(\max)} - K_1 [V_{ref} - v_{ss}] - K_4 \int [V_{ref} - v_{ss}] dt \\ + K_2 i_{c2(\max)} - (K_3 - R_1) i_{L1(\max)} < v_s + v_{c1(\min)} \end{cases} \quad (7)$$

where $V_{e(\max)}$ and $V_{e(\min)}$ denote the maximum and minimum input voltages respectively; v_{ss} denotes the expected steady state output voltage which is basically a DC parameter of a small error from the desired reference voltage V_{ref} ; and

$i_{L1(\max)}$, $i_{L1(\min)}$, $i_{c2(\max)}$ and $i_{c2(\min)}$ are respectively the maximum and minimum inductor and capacitor currents when the converter is operating at full-load condition. $v_{c1(\min)}$ denotes the minimum voltage of capacitor C_1.

The stability of the converter under the controller can be achieved by making the eigenvalues of the Jacobian matrix of the system to have negative real parts.

For FPGA implementation, simplification of the control algorithm can reduce logic resource consumption. As the steady-state errors in the ISMC are mainly reflected in the output voltage, so a simplified DISMC which includes only integral voltage control is proposed.

$$s = \beta_1 e_1 + \beta_2 e_2 + \beta_3 \int e_1 dt + \beta_4 \int\int (e_1 dt) dt \qquad (8)$$

The corresponding sliding surface is relatively straight forward with ignorance of the integral of current. The equivalent control expression becomes:

$$\begin{cases} \rho = \dfrac{1}{v_{c1} + v_s} [K_1 (V_{ref} - v_s) + K_3 \int (V_{ref} - v_s) dt \\ -K_2 i_{c2} + R_1 i_{L1} + (v_{c1} + v_s - v_e)] \end{cases} \qquad (9)$$

From (9), it can be seen that only three parameters are needed to turn.

Simulations using SEPIC hybrid model have been made. The comparison waveforms between DISMC (DISM1) and simplified DISMC (DISM2) for reference voltage change (0 to 14V) and a step load changes between 20Ω and 13.3Ω is shown in Fig. 2.

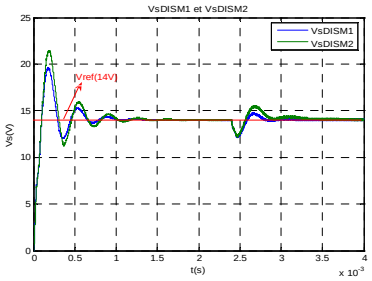


Fig. 2 Simulation response for a reference voltage change (0 to 14V) and a load step variation from 20Ω to 13.3Ω at 0.0024s

The simulation results show that the DISMC display excellent large-signal property (a major feature of the SMC) of having a response for load changes. It can be seen that there are not steady-state errors for both controls. The lack of current item control induces more overshoot but the dynamics remains acceptable.

IV. EXTENDED KALMAN FILTER

As the proposed controls require the knowledge of all the states, the use of sensors poses a technological burden especially in embedded systems, on the one hand, some sensors might not be relatively precise (noisy) such as current sensors, and on the other, their integration might increase the cost and the system size [21].

The traditional observers like Luenberger are easy to design, but only converge locally. Sliding mode observers can be designed as in [22]. However, load variation is not taken into account. Moreover, these observers are based on continuous time model. An Euler method is generally used to discretize the observers on a digital form [23]. For a FPGA implementation, a discrete-time observer designed by a discrete-time model is preferable.

Therefore, an extended Kalman observer taking into account the load variation is developed. By choosing the states vector as $[i_{L1} \quad v_{c1} \quad i_{L2} \quad v_s \quad R]^t$, the model (2) can be written:

$$x_k = f(x_{k-1}, u_{k-1}, w_{k-1}) \qquad (10)$$

With measurement of v_s that is

$$y_k = h(x_k, v_k) \qquad (11)$$

The random variables w_k and v_k represent the process and measurement noise (respectively). The noise covariance matrixes are defined as follows:

$$Q = \mathrm{cov}(w) = E(w, w^t) \qquad (12)$$

$$R = \mathrm{cov}(v) = E(v, v^t) \qquad (13)$$

Define matrix P as the error covariance of state estimation:

$$P_k = E\left\{e_k \cdot e_k^t\right\} = \sum_{i=1}^{5} \left\{\left[x_i - \hat{x}_i\right] \cdot \left[x_i - \hat{x}_i\right]^t\right\} \qquad (14)$$

E{.} is the computation of expectation value.

The EKF is then derived by the following iteration:

1) Linearization of (10) and (11)

$$\begin{cases} x_k = A_{k-1} x_{k-1} + B u_{k-1} + G \\ y_k = C x_{k-1} \end{cases} \qquad (15)$$

Where A is the Jacobian matrix partial derivatives of f with respect to x, G is a constant matrix.

2) Prediction of the state and covariance

$$\begin{aligned} \hat{x}_{k|k-1} &= A_{k-1} \hat{x}_{k-1|k-1} + B u_{k-1} + G \\ P_{k|k-1} &= A_{k-1} P_{k-1|k-1} A_{k-1}^T + Q \end{aligned} \qquad (16)$$

3) Computation of the Kalman gain

$$K_k = P_{k|k-1} C^t \left(C P_{k|k-1} C^t + R\right)^{-1} \qquad (17)$$

4) Update estimation with measurement

$$\hat{x}_{k|k} = \hat{x}_{k|k-1} + K_{k+1} \left(y_k - C \hat{x}_{k|k-1}\right) \qquad (18)$$

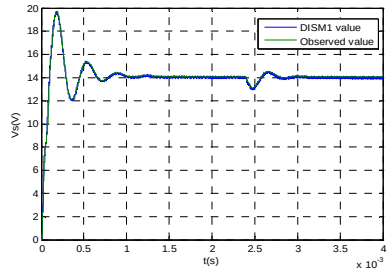
5) Update the error covariance matrix

$$P_{k|k} = P_{k|k-1} - K_{k+1} C P_{k|k-1} \qquad (19)$$

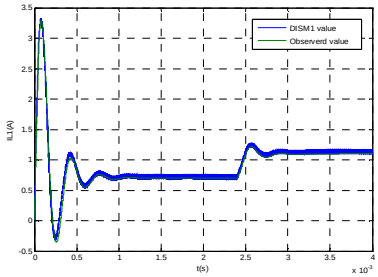
The covariance matrix Q and R are chosen to get the best trade off between stability and convergence time.

The SMC proposed in section III and the EKF are tested on simulation using the Simulink fixed-point toolbox of Matlab/Simulink. Indeed the controllers and the observer are computed with a fixed-point algorithm in order to keep the simulation condition close to practical implementation. Fig. 3 and 4 give some examples of the simulation results.

Figs. 3(a) and 3(b) show the waveforms of the measured value and the observed value with DISMC (DISM1) for a step reference change (0 to 14V) and a load step variation from 20Ω to 13.3Ω at 0.0024s.



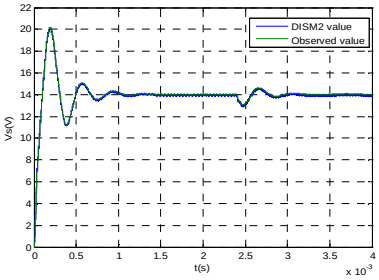
(a) Output voltage Vs



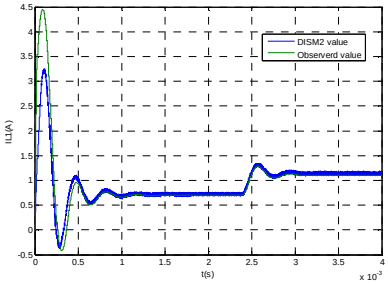
(b) Input current IL1

Fig. 3 Fixed-point simulation of the DISM1 controller of measured and observed value

In Fig. 4(a) and 4(b), the simplified DISMC (DISM2) waveforms of the measured value and the observed value are compared for the same simulation conditions.



(a) Output voltage Vs



(b) Input current IL1

Fig. 4 Fixed-point simulation of the DISM2 controller of measured and observed value

They show the quick convergence and the robustness of the proposed EKF against strong disturbance of the load value. With the effectiveness of this observer, DISMC can be implemented in the FPGA design.

V. FPGA IMPLEMENTATION

Experimental validations of the proposed DISM controllers are provided on a 10-100W SEPIC converter to validate the theoretical design. Fig. 5 shows the experimental setup of the SEPIC converter. The parameters are R_1=1.2Ω, R_2=0.8Ω, L_1=185μH, L_2=13μH, C_1=7.6μF, C_2=7.6μF, v_e=10-20V, v_s=14V, f_s=500kHz.

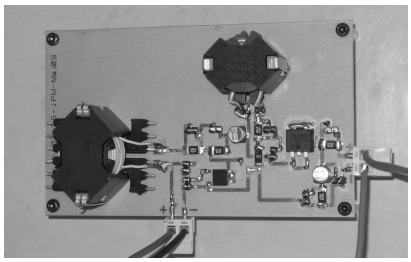


Fig. 5 500kHz prototype

The controllers and observer are implemented in fixed-point algorithmic calculation in VHDL on a Virtex-II Pro XC2VP30 board by Xilinx Inc. An Analog Device A/D converter ADS900 component is used for the output voltage measurement. A DPWM is required to convert the control signal to the variable duty cycle signals which drive the switches in the power stage. In order to eliminate undesirable limit-cycle oscillation, the DPWM resolution is required as the highest possible [24]. Unlike the DSP board where the PWM signals of interest is generated by DSP PWM core, in the FPGA implementation, a particular attention must be paid for the DPWM.

The main concern of high-frequency high-resolution DPWM is to generate signals to meet the output voltage accuracy which needs high frequency clock in the approach of counter-comparator based DPWM. They require significantly large power and unreachable high frequency clock that nullify most of the digital control advantages. For example, to perfume an 11-bit DPWM with the counter comparator block, an 11-bit DPWM is required. Thus for operation at switching frequency of 500kHz, the counter comparator block needs a $2^{11} \times 500k = 1.024GHz$ clock. This constraint limits the switching frequency on one hand and DPWM resolution on the other hand.

In this paper, a second-order Δ-Σ architecture [25][26] is adapted. Fig. 6 shows the proposed hybrid DPWM structure which is composed of an 8-bit Δ-Σ modulator and an 8-bit counter-comparator. For the first, only two adders are used, and with a truncator, three least significant bits (LSBs) and eight MSBs are generated, respectively. In addition, each delay block is realized with only 3-bit D flip-flops and the sizes of the adders are reduced accordingly. The ×2 multiplication block is implemented as a simple 4-bit logic shifter. The modulator is clocked at the switching frequency by a signal created with the core DPWM. For the 8-bit counter-comparator, by comparing counter value and the output of the 8-bit Δ-Σ modulator, the switch of the converter is turned on/off via an R-S latch.

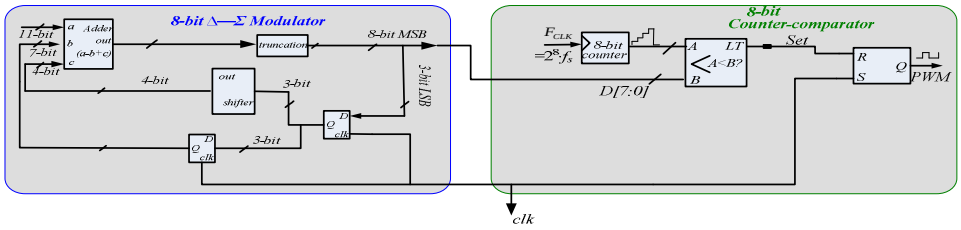


Fig. 6 Proposed 11-bit FPGA-based Error-feedback DPWM acts as 8-bit Δ-Σ modulator, 8-bit counter comparator

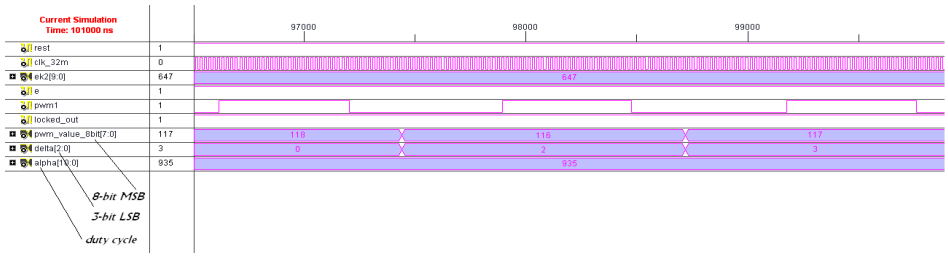


Fig. 7 Timing-simulation waveforms of the 11-bit DPWM

The timing-simulation for the complete 11-bit FPGA-based DPWM is shown in Fig. 7 with an example ratio of 935, which is equal to D[10:0]="01110100111". As it is shown, the multi-bit Δ-Σ DPWM can effectively achieve 11-bit resolution at high-frequency through only an 8-bit hardware Core DPWM, which dramatically reduces the power consumption of DPWM module. Thus for operation at f_s=500kHz switching frequency, the counter comparator block merely needs a $2^8 \cdot f_s = 128MHz$ clock instead of the $1.024GHz$ clock of the classical counter-comparator DPWM. Fig. 8 summarize the diagram block of the FPGA based SMC controller (indirect SMC algorithm, EKF and Hybrid DPWM).

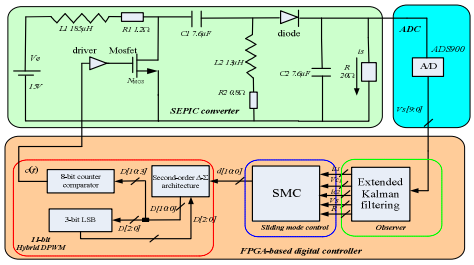


Fig. 8 Diagram block of the test platform for digitally-controlled SMPS

Fig. 9 and Fig. 10 show the experimental output voltage Vs transient response using the proposed DISM1. It can be seen that when the SEPIC is in steady-state operation condition, the controller maintains the deserved output voltage (14V). In transient operation condition when the load suddenly varies from 0.7A to 1.08A (20Ω to 13.3Ω), the controller can quickly regulate the output. The result shows that the transient response time is small and the offset on the output voltage is almost 400mV, i.e. 3% of the output voltage (14V). The experimental results confirm the simulation results obtained in section III.

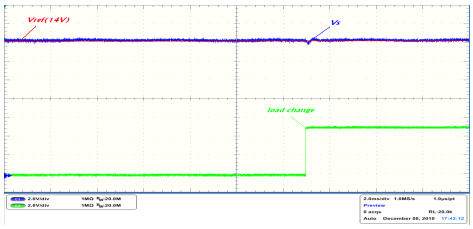


Fig. 9 Response of Vs with DISM1 when load changes from 0.7A to 1.08A

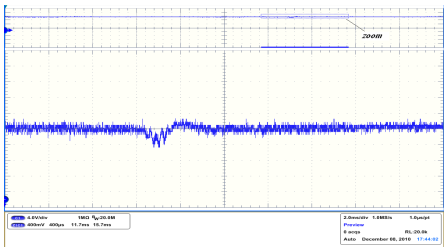


Fig. 10 Zoom of output voltage response

The experimental output voltage Vs transient response with the proposed DISM2 is shown in Fig. 11 and Fig. 12. DISM controller without the integral of current are performed for the same load variation. The lack of current item control brings more overshoot and oscillation as previously underlined with the simulation results.

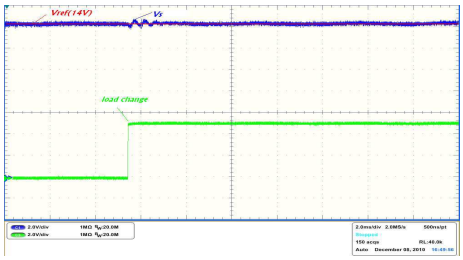


Fig. 11 Response of Vs with DISM2 when load changes from 0.7A to 1.08A

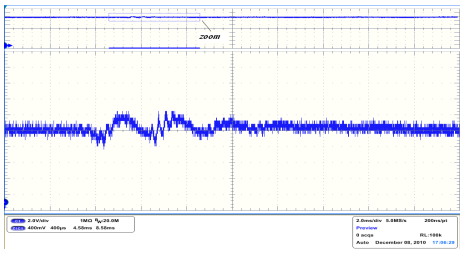


Fig. 12 Zoom of output voltage response

VI. CONCLUSION

SEPIC is a good candidate for a universal DC-DC power supply. Sliding Mode Control was applied in order to provide a fast and stable control law for the SEPIC which is not widely used due to the limited control studies being carried out on. In this paper, a double integral sliding mode control scheme in the indirect form is introduced. It has been found that the proposed control strategies provide satisfying static and dynamic performances, and at the same time, are not complicated to design. Experimental results have been conducted on a FPGA platform to validate the different controllers. The FPGA implementation is particularly interesting since all proposed modules (DPWM, SMC, Kalman observer) could be implemented in ASIC to potentially achieve high integrated power supply.

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